RESEARCH ARTICLE OPEN ACCESS

Dual Edge Triggered Phase Detector for DLL and PLL Applications

Prasanna Kumar L[1], Ashok S[2], Arun Kumar N[2]
1 - PG Student, 2 – Asst. professor, Veltech Multitech Dr. RR Dr.SR Engineering College

Abstract–
An ASIC design of Dual Edge Triggered Phase Detector(DET PD) for Delay locked loop(DLL) and Phase locked loop(PLL) applications is proposed in this paper.The proposed DET PD has high locking speed and less jitter. The designs are based on TSPC flip flop logic, which overcomes the issue of narrow capture range. The Double edge triggered phase detector dissipates less power than conventional designs and can be operated at a frequency range of 250MHz to 1GHz.The proposed DET-PD is designed using 180nm CMOS process technology at a 1.8V supply voltage in cadence virtuoso and circuit simulated in cadence spectre.
Keywords: *–ASIC, DLL, DET PD,TSPC*

I. INTRODUCTION

Phase locked loops (PLL) and Delay locked loop (DLL) are broadly used in high-speed systems, communication systems, frequency synthesizers, RAM, clock synchronization and data recovery circuits[1]-[6]. With the recent fast growth in digital devices the clock generation and distribution as become very important constraint. The PLL and DLL plays major role to achieve the required clock generation and distribution. A Phase Locked Loop (PLL) circuit synchronizes an input waveform within a selected frequency range, returning an output voltage proportional to variations in the frequency of input signal, hence,used to create a steady output frequency signals from a static low-frequency signal. The Phase Locked Loop comprises ofPhase Detector, Charge Pump, Loop Filter, Voltage Controlled Oscillator (VCO) and FrequencyDivider.

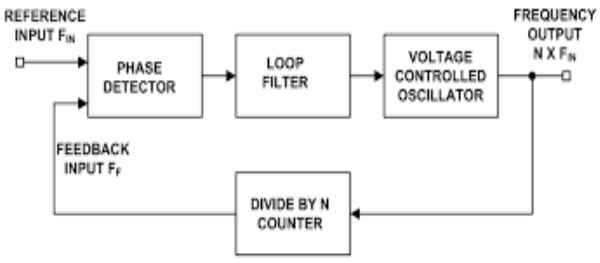

Fig 1. PLL Block Diagram

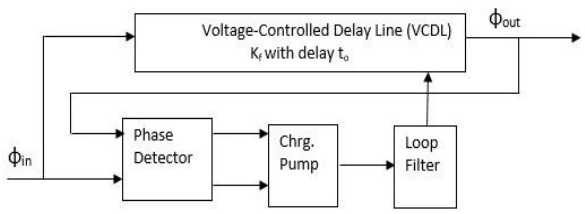

Fig 2. DLL Block Diagram

DLL was then developed to overcome the problem of jitter accumulation in PLL due to VCO. The DLL comprises of same components as that of PLL except the VCO was replaced by voltage control delay line (VCDL). Compared to PLL, DLL is simple to design with first order system, more stable and less jitter accumulation, while PLL is higher order system and more unstable [7].

In both cases, Phase detector plays a vital role which detects the phase differences between the reference clock and output clock in the loop and the resultant error voltage is produced.The phase detector has a great impact on the performance of DLL and PLL likejitter performance, locking speed and loop stability than other components.In clock generation and synchronization applications the lock speed need to be fast to achieve proper operation and preventing process stalling.The lock speed can be accelerated by increasing the gain of delay cell for dll and vco for pll, charge pump current. But this methods degrades the stability and jitter [8][9].The other way to speed up the lock speed without degrading the stability is Dual Edge Triggering concept [10] [11]. In this paper a new Dual Edge Triggered Phase detector has been proposed with low power, wider capture range and fast lock speed.

II. CIRCUIT DESCRIPTION

A D-FLIP FLOP TYPE PHASE DETECTOR

The basic role of phase detector is to compare the phase of the VCDL output to that of the reference signal and produce an error voltage that is fed to charge pump. Charge pump varies the amount of charges supplied to the VCDL according to the phase difference detected by PD. Phase detector is of various types. There are two types of phase detectors level sensitive phase detector and edge sensitive phase detector. The example of level sensitive phase detector is XOR PD. The most commonly used edge

sensitive phase detector is the D-flip flop type phase detector shown in below figure.

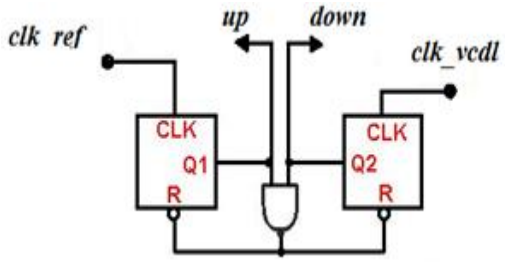

Fig 3. D-Flip Flop Type Phase Detector

The circuit uses two D-flip flops where the reference and VCDL signals which has to be compared enters the clock inputs. The two flip flops gives UP and DOWN signals which are given to the NAND gate and its output is fed to the inputs of both D-flip flop named as reset R.

The phase detector has probability of being at four states:

i. UP → 0 and DOWN → 0.
ii. UP → 1 and DOWN → 0.
iii. UP → 0 and DOWN → 1.
iv. UP → 1 and DOWN → 1.

When both UP and DOWN is at 1, AND gate gives "1" and both the flip flops gets reset. The phase detector may be single edge triggered or dual edge triggered.

III. PROPOSED ARCHITECTURE

A. SINGLE EGDE TRIGGERED PHASE DETECTOR

The modest flip-flop designs are single edge-triggered, samplingdata on only one clock edge, either the positive or negative edge. The single edge triggered phase detector detects the phase difference between two signals in only one clock edge. The loop gets updated at either rising edge or falling edge of the reference clock. The proposed single edge triggered phase detector is designed using True Single Phase Clock (TSPC) logic flip flop [12]. TSPC logic decreases the transistor count and the clock load is deduced to half. Flip-flops with TSPC logic operates with less power and at a higher speed. The Schematic of TSPC logic Positive edge triggered phase detector is shown in Fig 4.

It detects the phase differences only at positive edges. The reset path here is made up of NOR gate. Therefore, the flip flops gets reset when both UP_{PET} and $DOWN_{PET}$ are "0".

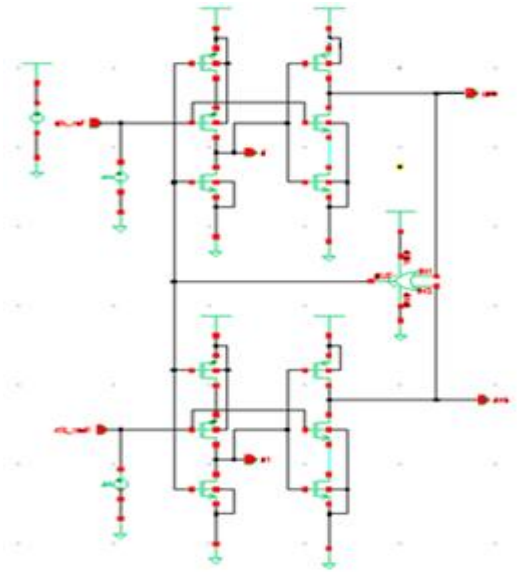

Fig 4. Positive Edge Triggered Phase Detector

TSPC logic of Negative edge triggered phase detector is shown in Fig 5. NET-PD detects the phase error in negative edges of the reference and feedback signals. Herein, OR gate is used as reset path which resets the circuit when UP_{NET} and $DOWN_{NET}$ signals are both "0".

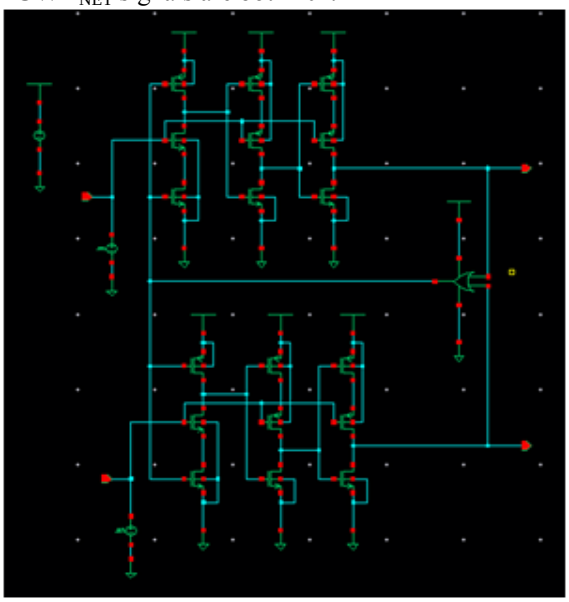

Fig 5. Negative Edge Triggered Phase Detector

B. DUAL EDGE TRIGGERED PHASE DETECTOR

The lock performance can be improvedby comparing the signals at both edges positive and negative edges of reference signal and output of feedback signal. This can be done by Dual edge triggered phase detector. An ideal DET PD achieves same throughput with half the clock frequency compared to Single edge triggered phase detector.It effectively reduces the power consumption in the clock distribution network.

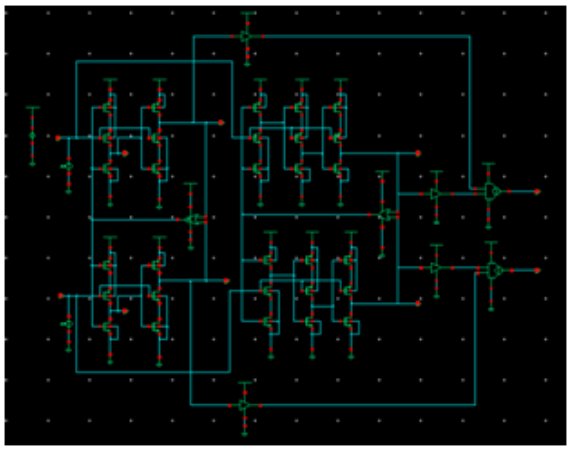

Fig 6a. Dual Edge Triggered Phase Detector

The clock distribution network makes up a great part of DLL such that substantial overallpower conservation is possible in DLL. The Dual edge triggered phase detector is designed by combining the two SET PD i.e. positive edge triggered and negative edge triggered phase detectors with pulse merging circuit. The DET PD is also designed using TSPC logic which reduces the area effectively. The pulse merging circuit uses two NAND gates. One NAND gate combines UP_{PET} and UP_{NET} to UP as of DET PD and similarly second one to combine $DOWN_{PET}$ and $DOWN_{NET}$ as DN of DET PD. The gain of the DET PD is linear in the range $-0.5T_{ref}$ to $+0.5T_{ref}$ and constant gain in region $0.5T_{ref}$ to T_{ref}, $-0.5T_{ref}$ to T_{ref}.The schematic of dual edge triggered phase detector is shown in Fig 6a and Fig 6b shows its gain characteristics[4].

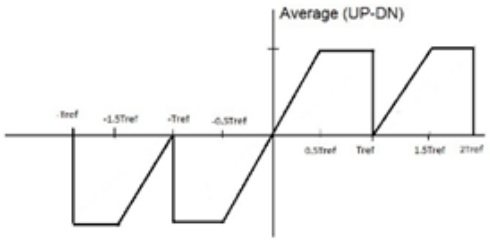

Fig 6a. Gain Characteristic of DET PD

IV. SIMULATION RESULTS

TSPC logic based Single edge triggered phase detector and Dual edge triggered phase detector is designed in Cadence Virtuoso 180nm cmos process technology with 1.8V supply voltage and simulated in Cadence Spectre. Fig.7aand Fig.7b shows the waveforms of positive edge triggered phase detector and negative edge triggered phase detector respectively at 1GHz frequency. Reference clock leads VCDL clock by 45°.

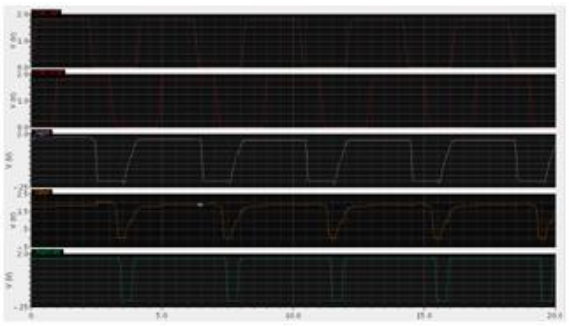

Fig 7a. Positive Edge Triggered Phase Detector Waveform

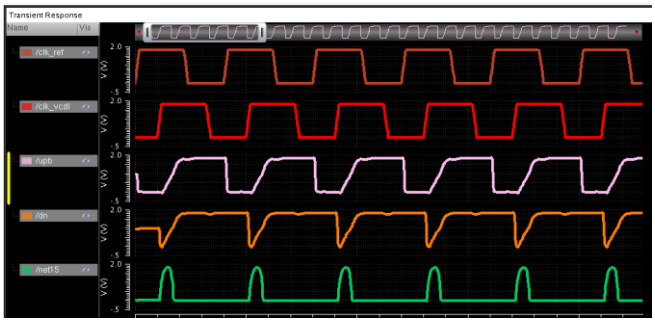

Fig 7b. Negative Edge Triggered Phase Detector Waveform

Since this is an edge triggered operation, phase detector outputs does not rely on the duty cycle of the input signals. But, in the case of DET PD, the edge sensitivity of the positive and negative edge triggered phase detectors have to be fixed to remove the multiple lock positions while pulse merging their outputs. The dead-zone problem ensues when the rising edges of the two clocks to be compared are very adjacent and it is the minimum pulse width of the phase detector output that is needed to turn on the charge pump completely.In the proposed design,reset pulses gets slender in the phase locked region to ease the dead zone problem which providessufficient time for the UP and DOWN signals to make the charge pump switch completely for very small phase differences.
The simulated graph of Dual edge triggered phase detector is shown in Fig 8.

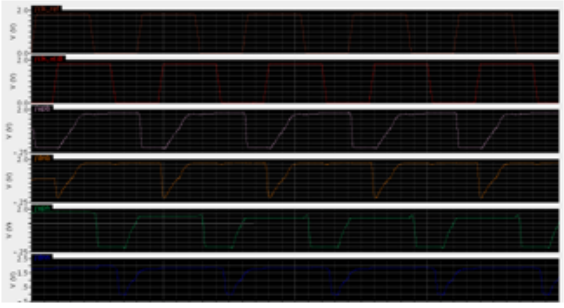

Fig 8. Dual Edge Triggered Phase Detector Waveform

V. PERFORMANCE COMPARISON

The performance comparison of the proposed design of single edge triggered phase detector and dual edge triggered phase detector with [1] is explained in Table 1.

TABLE 1 Performance Comparison

	[11]		This Paper	
PARAMETER	SET PD	DET PD	SET PD	DET PD
PROCESS	0.18µm CMOS		0.18µm CMOS	
SUPPLY VOLTAGE	1.8V		1.8V	
OPERATING RANGE	400-800 MHz		250MHz-1GHz	
POWER DISSIPATION	16mW	19mW	0.6mW	1.3mW

VI. CONCLUSION

This paper compares the performance of single edge triggered phase detector and dual edge triggered phase detector. The power consumption was reduced to 100.4uW and 390.9uW than conventional design where the power consumption is 16mW and 19mW for SET PD and NET PD respectively in clock distribution network. Because the clock distribution network has huge contribution to DLL, there is a significant fall in overall power dissipation of DLL. The proposed designs operate at maximum 1GHz with 1.8V supply voltage. Hence the clock speed of DLL is also increased meritoriously.

REFERENCES

[1] V. R. von Kaenel, D. Aebischer, C. Piguet, and E. Dijkstra, "A 320 MHz,1.5mW @ 1.35 V CMOS PLL for microprocessor clock generation,"*IEEE J. Solid-State Circuits*, vol. 31, pp. 1715–1722, Nov. 1996.

[2] I. W. Young, J. K. Greason, and K. L. Wong, "A PLL clock generatorwith 5 to 110 MHz of lock range for microprocessors," *IEEE J. Solid-State Circuits*, vol. 34, pp. 1599–1607, Nov. 1992.

[3] K. Kurita, T. Hotta, and N. Kitamura, "PLL-based BiCMOS on-chipclock generator for very high-speed microprocessor," *IEEE J. Solid-State Circuits*, vol. 26, pp. 585–589, Apr. 1991.

[4] D. W. Boerstler, "A low-jitter PLL clock generator for microprocessors with lock range of 340–612 MHz," *IEEE J. Solid-State Circuits*, vol. 34, p. 513, Apr. 1999.

[5] G. Chien and P. R. Gray, "A900-MHz local oscillator using a DLL-basedfrequency multiplier technique for PCS applications," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1996–1999, Dec. 2000.

[6] F. Lin, J. Miller, A. Schoenfeld, M. Ma, and R. J. Baker, "A register-controlled symmetrical DLL for double-data-rate DRAM," *IEEEJ. Solid-State Circuits*, vol. 34, no. 4, pp. 565–568, Apr. 1999.

[7] Chulwoo Kin, In-Chul Hwang and Sung-Mo kang, "A Low Power Small-Area ±7.28-ps-Jitter-1GHz DLL-Based Clock Generator," *IEEEJ.Solid-State Circuits*,vol 37, no.11, pp 1414-1420, nov-2002.

[8] BehzadRazavi, Design of Analog CMOS Integrated Circuits, Tata Mcgraw Hill 2002

[9] R Jacob Baker, Cmos: Circuit Design, Layout, and Simulation. IEEE Press series on Microelectronic systems.

[10] S.I. Ahmed and R.D. Mason, "A dual edge-triggered phase-frequency detector architecture." in *Int.Symposium on Circuits and Systems*, 2003, pp.721-724.

[11] KyunghoRyu, Dong-Hoon Jung, andSeong-Ook Jung, "A DLL With Dual Edge Triggered Phase Detector for Fast Lock and Low Jitter Clock Generator*" IEEE J on Circuits and Systems – I* regular papers vol 59, no.9,pp 1860-1870, Sep-2012.

[12] J. S. Wang, "A New True-Single-Phase-Clocked Double Edge Triggered Flip-Flop for Low-Power VLSI Design", in Proceedings of *IEEE International Symposium on Circuit and Systems*, pp. 1896-1899, 12 June 1997